ABSTRACT OF THE DISCLOSURE

An evaluation circuit 16 repeats processing in which an output VD thereof is reset, there is obtained repeatedly given times a difference between sampled output voltages Vo of a replica circuit 11R when respective times t1 and t2 have elapsed after a voltage Vi is step-inputted to the replica circuit 11R, and the differences are successively summed. A comparator circuit 20 compares a difference cumulation voltage VD with a reference voltage VS. A bias adjustment circuit 15 steps up the bias currents of the replica circuit 11R and an adjusted circuit 11 at every this given times if VD > VS, and ceases the adjustment if VD < VS.